REFERENCE CLOCK SETUP AND OPERATION

If the DCXO is not used, an external reference clock needs to be ac-coupled to XTALN (Pin M12). XTALP (Pin M11) is not connected (leave floating). The clock frequency must be between 5 MHz and 320 MHz, and can be scaled by 1×, ½×, ¼× and 2× using BBPLL, Rx and Tx reference dividers. The valid frequency range for the RFPLL phase detectors is 10 MHz to 80 MHz, and the scaled frequency of the reference clock must be within this range. For optimum phase noise it is recommended to operate the scaled clock as close to 80 MHz as possible. The selection between DCXO and external reference clock is made in the ad9361_init function.

The level for the clock should be 1.3 V p-p maximum(lower swings can be used but will limit performance). This signal can be a clipped sine wave or a CMOS signal. The best performance will be seen with the highest slew rate possible.

The XTALN (Pin M12) has an input resistance of ~ 10 kΩ in parallel with 10 pF.

PHASE NOISE SPECIFICATION

The AD9361 Rx and Tx RFPLLs use the DCXO or external clock as their reference clock as well. For this reason, it is extremely critical that the crystal or clock source have very low phase noise. The recommended phase noise specification is shown in Figure 2.

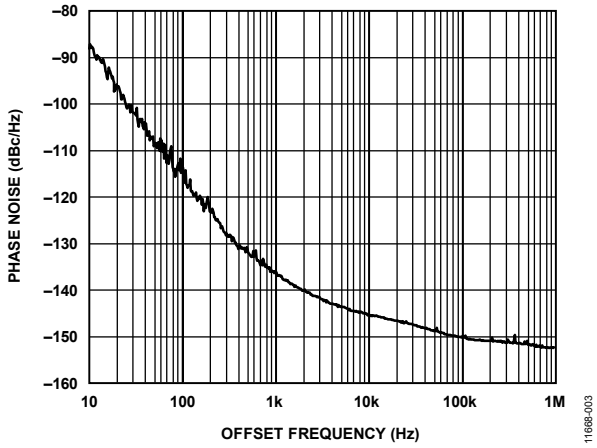

Figure 2. Phase Noise vs. Offset Frequency