Chapter 5 Architecture Overview

The USB3320 consists of the blocks shown in the diagram below. All pull-up resistors shown in this diagram are connected internally to the **VDD33** pin.

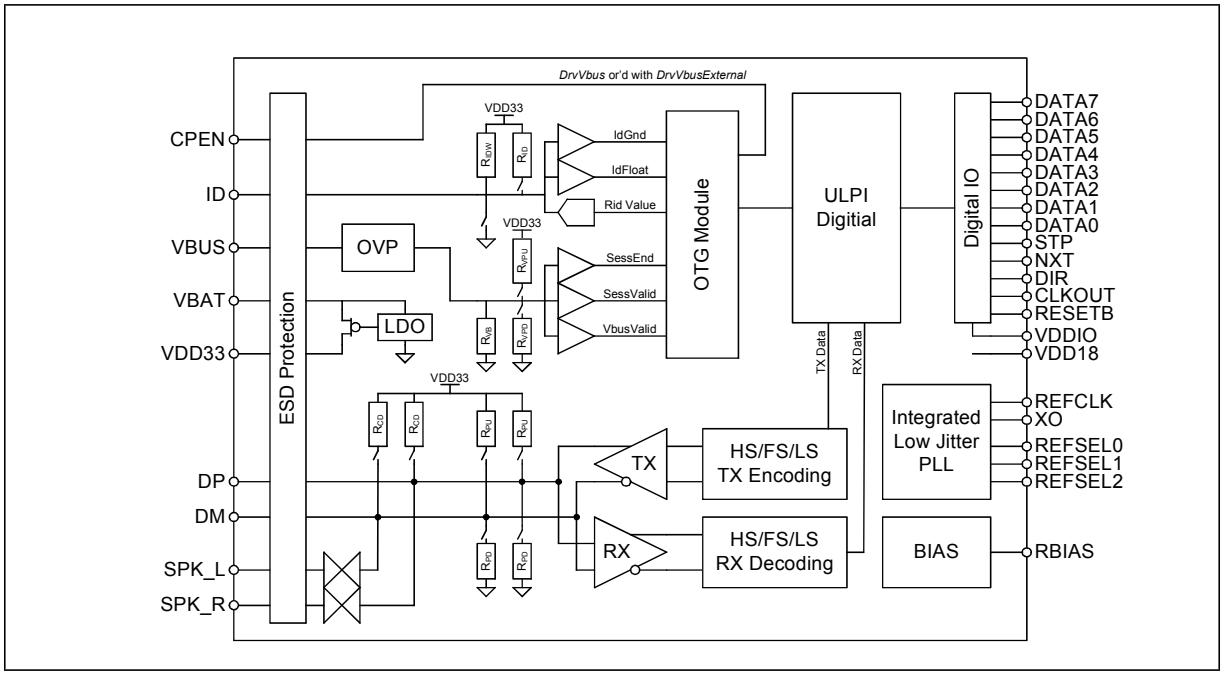

Figure 5.1 USB3320 Internal Block Diagram

5.1 ULPI Digital Operation and Interface

This section of the USB3320 is covered in detail in Chapter 6, ULPI Operation.

5.2 USB 2.0 Hi-Speed Transceiver

The blocks in the lower left-hand corner of Figure 5.1 interface to the DP/DM pins.

5.2.1 USB Transceiver

The USB3320 includes the receivers and transmitters that are compliant to the Universal Serial Bus Specification Rev 2.0. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The RX block consists of a differential receiver for HS and separate receivers for FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

Data from the TX Logic block is encoded, bit stuffed, serialized and transmitted onto the USB cable by the TX block. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB3320 TX block meets the HS signalling level requirements in the USB 2.0 Specification when the PCB traces from the **DP** and **DM** pins to the USB connector have very little loss. In some systems,

it may be desirable to compensate for loss by adjusting the HS transmitter amplitude. The *Boost* bits in the HS TX Boost register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins.

5.2.2 Termination Resistors

The USB3320 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω high speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the transceiver when operating in synchronous mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration. The possible valid resistor combinations are shown in Table 5.1, and operation is guaranteed in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not guaranteed and the settings in the last row of Table 5.1 will be used.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM high speed termination resistors

The USB3320 also includes two **DP** and **DM** pull-up resistors described in Section 5.8.

Table 5.1 DP/DM Termination vs. Signaling Mode

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3320 TERMINATION RESISTOR SETTINGS				
	XCVRSELECT[1:0]	TERMSELECT	OPMODE[1:0]	DPPULLDOWN	DMPULLDOWN	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or VBUS < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host Hi-Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b