DATA SHEET

Confidential

RDA5815

Fully Integrated, Direct Down-Conversion Satellite Receiver for DVB-S,DVB-S2&ABS-S,MMDS

Update History

Rev	Date	Author	History Description
2.0	2011-6-8	Wang hongxin	The primary datasheet for B version chip

RDA Microelectronics, Inc.

RDA5815-Fully Integrated Satellite receiver for DVB-S , DVB-S2 & ABS-S，MMDS

Features

- Single-chip RF-to-baseband Satellite receiver

- CMOS Fully integrated RF front end

- Low noise and wide dynamic range zero-IF receiver

- Input frequency range: 250 to 2300 MHz

- Input signal level: -100 to 5 dBm

- More than 85dB gain control range

- Fully integrated PLL (dividers, charge pump, phase & frequency detectors, loop filters, etc.)

- Integrated RX VCO

- Integrated baseband LPF with selectable cut-off

frequency from 4MHz to 40MHz with 1MHz step

- Integrated LNA with RF AGC

- Integrated reference oscillator (27MHz is defult)

- I^2C bus interface

- Automatic gain control

- 0.11µm RF CMOS technology

- 3V to 3.6V operation

- power consumption of less than 600mW

- Lower profile packages:

  ➢ RDA5815 5×5 mm QFN32
  Pin assignment (32 pin QFN 5×5 mm)

Applications

- Set-top boxes

- Digital video recorders

- Digital television

- Satellite PC-TV

- SMATV trans-modulators (Satellite Master Antenna TV)
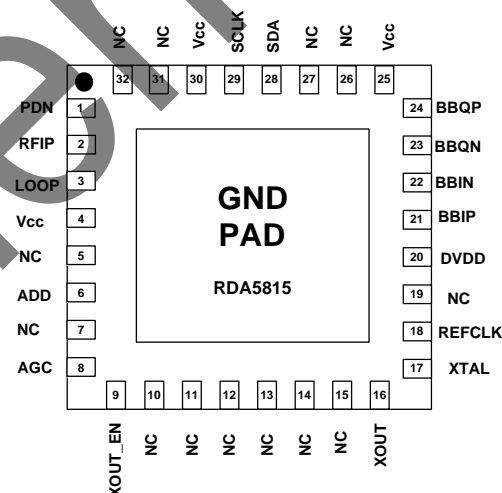

General Description

The RDA5815 is a fully integrated direct conversion

RF front end for DVB-S,DVB-S2&ABS-S,MMDS digital satellite

Reception standard CMOS process. The receiving frequency range is from 250MHz to 2300MHz, and the baseband filter's bandwidth can be selected from 4MHz to 40MHz with 1MHz step.

The rda5815 consists of a variable gain LNA, quadrature downconverter, variable IF gain amplifiers, variable low-pass filters, reference oscillator, VCOs, synthesizer and output baseband amplifier to drive external ADC.

Based on RDA's some innovative technique, the rda5815 offers excellent phase noise and very low implementation loss, required for advanced modulation systems such as 8PSK and DVB-S2. This tuner RF IC does not require a balun and its fully integrated design saves valuable board space and simplifies RF layout.

Functional Block Diagram
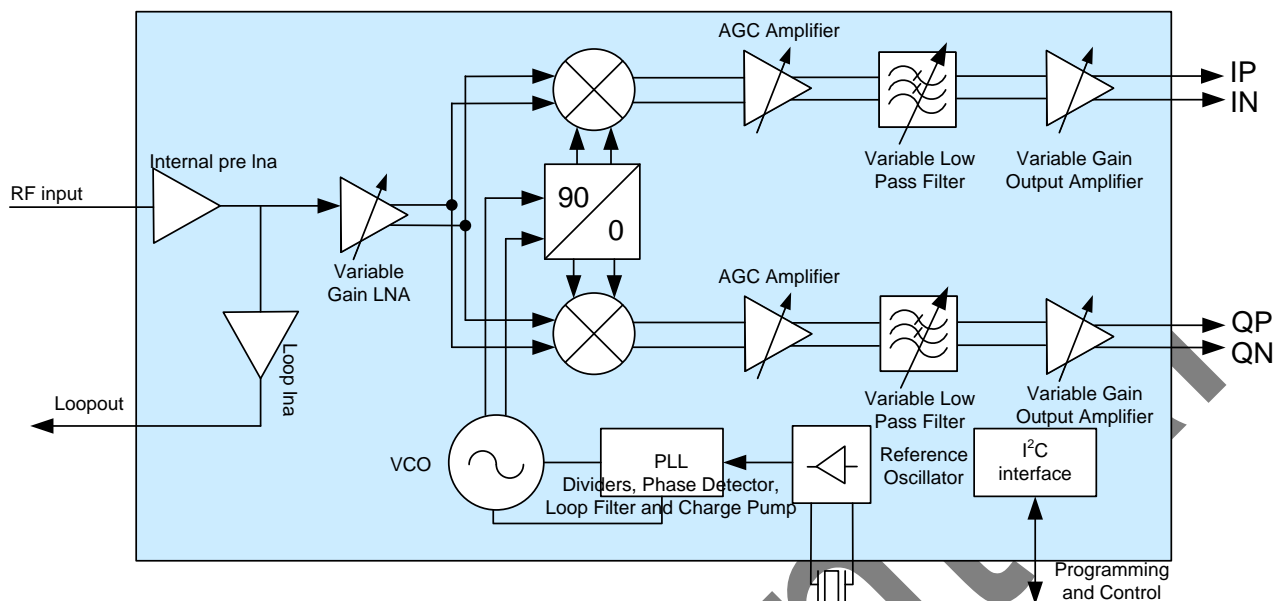
Functional Description

The loop lna is used to generate the loopout signal.An on chip variable gain LNA is used to provide wide tuner dynamic range. A direct conversion architecture is used to convert the RF signal to in-phase and quadrature baseband signals. The signals required for direct conversion are all generated within the chip by a fully integrated PLL and a quadrature LO generator. The frequency of the VCO is set by internal PLL circuits, which are programmable via a 2-wire (I^2C) serial bus. The LO signals are mixed with the RF signal input and then filtered by low-pass filters to remove the upper image produced by the mixer. A variable gain amplifier is then used to adjust the baseband signal levels before processing by the channel selection filters to optimize noise performance and prevent distortion within the filters. The channel select filters are digitally programmable low pass filters with 1MHz step from 4MHz to 40MHz. The output amplifier buffered the signal from the filters to increase the driving capability to the next baseband ADC.

Some innovative technique is used to correct and alleviate DC offsets inherent in direct conversion mixers, the channel select filters and output buffers.

Loopout   LNA

The loopout lna is used to generate the loopout signal.

Variable Gain LNA

This stage receives a signal from the LNB through external matching circuit, the input resistance is matched to 75Ω coaxial cable. The gain can be programmed with the 2-wire (I^2C) interface to insure wide dynamic range of the receiver.

AGC Amplifier

The AGC Amplifier receives the IQ signals from the quadrature mixer then amplifies them and sends to the base band low pass filter. The gain is also programmed and controlled by the 2-wire (I^2C) interface.

Baseband LPF

The bansband low-pass filter is designed to have variable cut-off frequency. The bandwidth of the LPF is selectable from 4MHz to 40MHz with 1MHz step. The DC-offset calibration can be carried out controlled by the interface. A innovative technique ensure the filter's bandwidth variety within 5%.

Reference Oscillator

The oscillator is on-chip integrated and both the crystal and crystal oscillator are supported. The 27MHz is recommended. The centre oscillation frequency can be adjusted accurately with the XAFC pin (optional function).

VCO

The receiver integrates two VCOs which ensure covering the full receiving frequency from 250MHz to 2300MHz. The two VCOs can be switched between each other with relevant register and the VCO's band is programmed using 2-wire (I^2C) interface. The first VCO oscillates from 2100MHz to 2918MHz, the second oscillates from 2818MHz to 4350MHz. After divided by two or four, lo signal from 900MHz to 2250MHz can be obtained.

LO frequency	Used VCO	Divider
950MHz~1074MHz	VCO2	4
1075MHz~1434MHz	VCO1	2
1435MHz~2150MHz	VCO2	2

PLL

The fractional-N frequency synthesizer use 27MHz reference as default. The dividers, loop filters, phase&frequency detector, charge pump are all integrated on chip.

Baseband Output Amplifier

Class-AB architecture is selected for the output buffer, this makes it more flexible to the next Baseband solution's input load. The gain of this stage can also be programmed with interface to farther increase the receiver dynamic.

XOUT Output

The XOUT pin can supply the reference clock for baseband chip, which is controlled by the XOUT_EN pin and the XDIV2_EN pin. The XOUT pin sends out signal when XOUT_EN is Vdd, and doesn't send out signal when XOUT_EN is GND. The output frequency is equal to xtal frequency when XDIV2_EN is GND, and is equal to (xtal frequency)/2 when XDIV2_EN is Vdd.

I^2C interface

The interface is the control unit of all the analog blocks, it is provided for configuration and monitoring all internal registers, the I^2C bus consists of two wires: serial clock line (SCL) and serial data line (SDA). The LNA's gain, AGC, baseband LPF's bandwidth, VCO's and crystal oscillator's current, VCO's oscillation frequency are all controlled by the 2-wire interface.
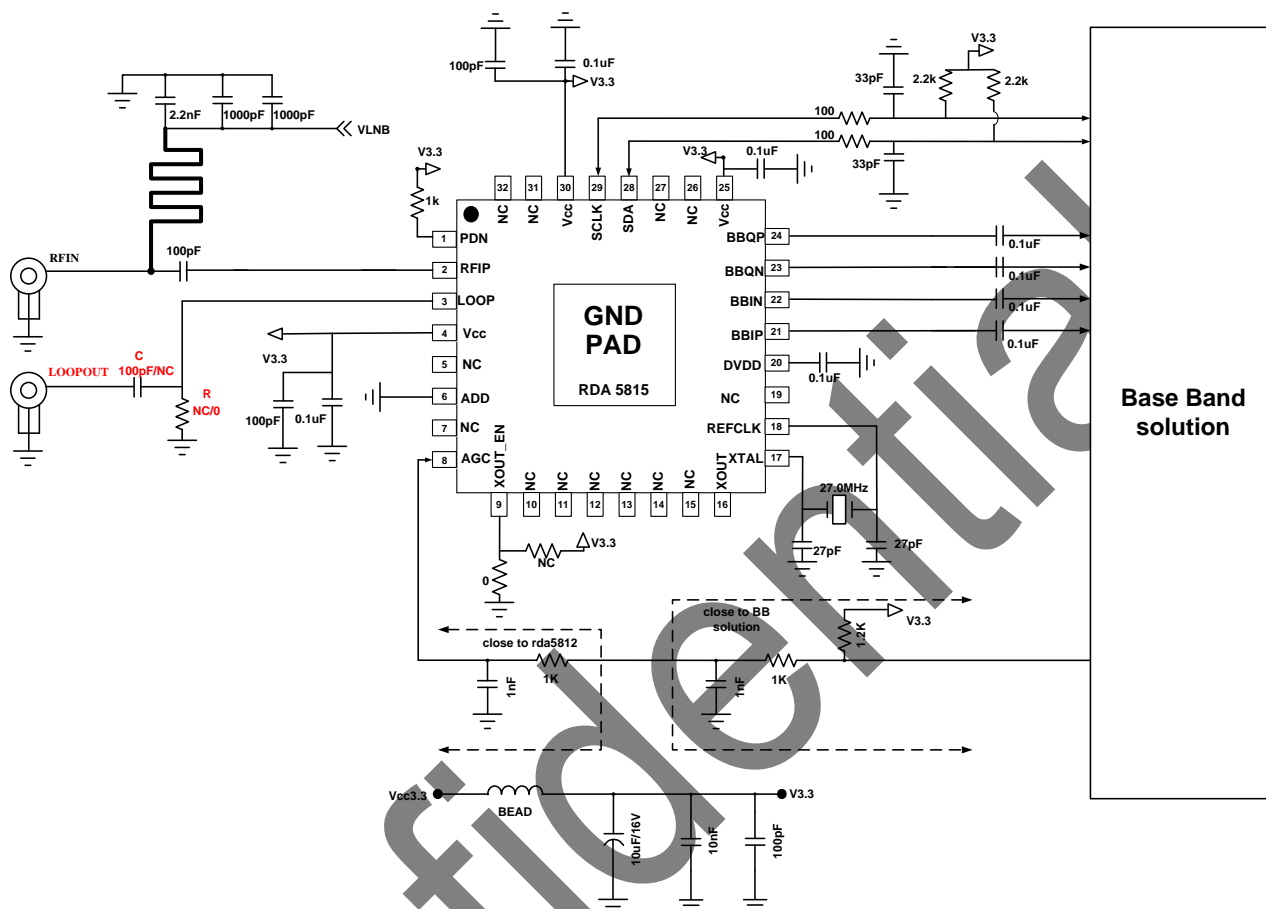
Direct AGC control

Through the AGC pin input, the receiver chain's gain can be directly controlled by the baseband solutions. The receiver gain changed inversely with the AGC control signal, this means that when AGC signal goes high, the receiver gain will drop to relevant level and vice versa.
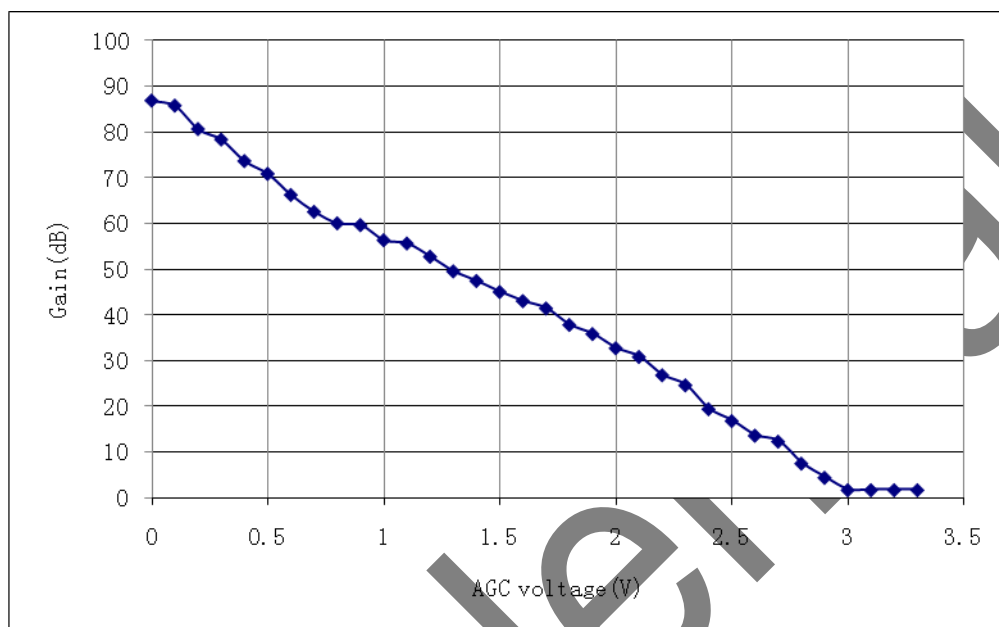
Typical application circuit

Application circuit

Note:

The 5815 support the loopout, the setting is as follows:

loopout	The third pin of 5815<loop>	The value of register 04H's 5bit
on	R=NC, C=100pF	0
off	R=0, C=NC	1

5bit of register 04H	rf_bypass_enable_b	0: power up 1: power down Default: 1'b0 The bypass buf functions at power-up of the chip by default. If this function is not required, set this bit to logic '1', which will save about 6mA current.

Pin Description
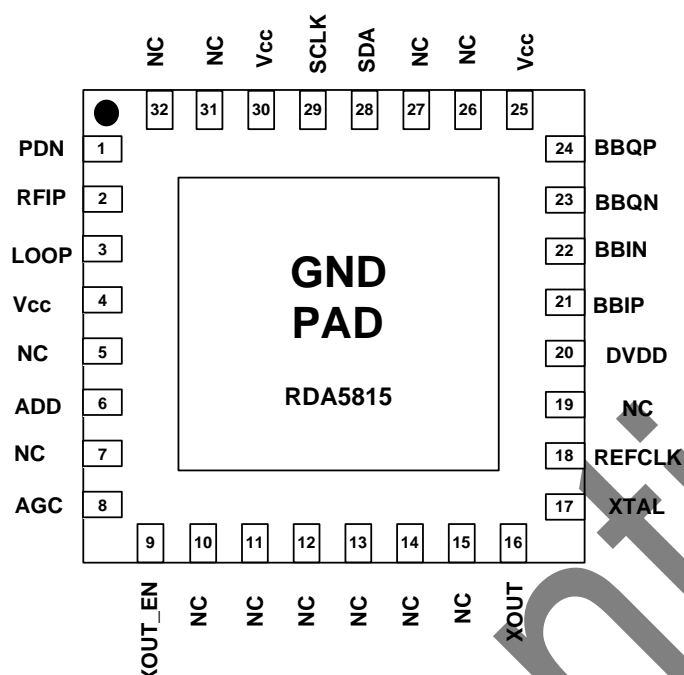
Pin number	Name	I/O	DESCRIPTION
1	PDN	I	Receiver power control. If low, Receiver total power down, including the crystal oscillator. If High, the chip is enabled.
2	RFIP	I	RF Positive Input
3	LOOP.		LOOPOUT
4	Vcc	I	Supply voltage for 5815. Connected to 3.3 V.
5	N.C.		Not connected.
6	ADD	I	I2C bus address selection terminal. Allowing the use of more than one device per I2C bus system by the voltage on this pin. See Table 7 for programming details.
7	N.C.		Not connected.
8	AGC	I	AGC control input from baseband solutions
9	XOUT_EN	I	To control the XOUT pin to send out the buffed xtal signal or not. If GND,XOUT=Off; If VDD,XOUT=On
10	N.C.		Not connected.
11	N.C.		Not connected
12	N.C.		Not connected
13	N.C.		Not connected
14	N.C.		Not connected
15	N.C		Not connected.
16	XOUT	I	Buffered Crystal oscillator output for BaseBand solution
17	XTAL	I/O	Connect to Crystal (27MHz is recommanded)

18	REFCLK	I/O	Connect to Crystal (if using external crystal oscillator, this pin connect to the oscillator's output)
19	NC		Not connected
20	DVDD	O	Output of the supply voltage for Digital, Connected to cap
21	BBIP	O	Negative Baseband Q Channel Out
22	BBIN	O	Positive Baseband Q Channel Out
23	BBQN	O	Positive Baseband I Channel Out
24	BBQP	O	Negative Baseband I Channel Out
25	Vcc	I	Supply voltage for 5815. Connected to 3.3 V.
26	NC	O	Not connected
27	NC	O	Not connected
28	SDA	I/O	Serial data input/output, connected to 3.3V with 10kΩ resistor
29	SCLK	I	Serial clock input
30	Vcc	I	Supply voltage for 5815. Connected to 3.3 V.
31	N.C.		Not connected
32	N.C.		Not connected

Electrical Specifications

Table 1   Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNIT
Analog Supply Voltage	AVDD	3	3.3	+3.6	V
Ambient Temperature	T_A	-25	27	+85	°C

Table 2   DC Electrical Specification

Parameter	Symbol	MIN	TYP	MAX	UNIT
CMOS Low Level Input Voltage	V_{IL}	0		0.3*VDD	V
CMOS High Level Input Voltage	V_{IH}	0.7*VDD		VDD	V
CMOS Threshold Voltage	V_{TH}		0.5*VDD		V

Table 3   Power consumption specification

(VDD =3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Symbol	Description	Condition	TYP	UNIT
ICC	Receiver on		170	mA
ICC()	tuner Disabled	PDN=1,Enable=0,Rxon=0	6	mA

Table 4   System Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency	f_{IN}		250		2300	MHz
Minimum RF input	RFIL	4.42MS/s, QPSK3/4,noise free		-97	-95	dBm
Maximum RF input	RFIH	4.42MS/s, QPSK3/4, noise free		5		dBm
Minimum RF input	RFIL	45MS/s, QPSK3/4, noise free		-87	-84	dBm
Maximum RF input	RFIH	45MS/s, QPSK3/4, noise free		5		dBm
Noise Figure	NF	Max Gain (Minimum AGC)		3.7	5	dB
Input refered third-order intercept	IIP3	Minimum Gain (Maximum AGC)		5	7	dBm
Input refered econd-order intercept	IIP2	Minimum Gain (Maximum AGC)	41	47	55	dBm
Gain flatness over frequency	GF	Input freq=900 to 2250MHz		3	4	dB
IQ amplitude balance	IQAB			0.2	0.5	dB
IQ phase balance	IQPB			0.3	0.5	Deg
Minimum voltage	Gv(min)	AGCIN set to maximum		4		dB

conversion gain		(3.3 V)				
Maximum voltage conversion gain	Gv(max)	AGCIN set to minimum (0.1V)		82		dB
Voltage conversion gain step	Gv(step)			0.2		dB
Matched input resistance	R_{IN}	After matching		75		Ω
Power up setting time	PUST			1		ms
Input reflection coefficient	S11	After matching		-8	-7	dB

Table 5   Frequency Synthesizer Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
t_{SW}	RX Switch on time			200		us
f_{RFLO}	synthesizer frequency		900		2250	MHz
PN1	Phase noise	Δf=1kHz		-85	-75	dBc/Hz
PN2		Δf=10kHz	-100	-95	-90	dBc/Hz
PN3		Δf=100kHz	-110	-105	-100	dBc/Hz
PN4		Δf=1MHz	-138	-133	-130	dBc/Hz

Table 6   Baseband LPF and Output Amplifier Characteristics

Parameter	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
3 dB baseband filter bandwidth	BBF(3dB)		4		40	MHz
Cutoff frequency accuracy at -3dB	FC				+/-5	%
LPF 2fc attenuation	LPF ATT1		25			dB
Flatness	FLTN			0.5	1	dBpp
Group delay	Td(g)			2		ps
Maximum differential output voltage		Clipping level		0.9*VDD		Vpp
Output common mode voltage			0.3*VDD	0.5*VDD	0.6*VDD	V
Differential Output offset voltage				30		mV
IQ output impedance			25	45	55	Ω
Output Amplifier minimum load impedance			1K			Ω
Output Anplifier maximum Load capacitance					10	pF

Table7   XTAL & XOUT Characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

Parameter	SYMBOL	MIN	TYP	MAX	UNIT
XTAL differential output voltage			680		mVpp
XTAL common mode voltage			0.55		V

Parameter	SYMBOL	MIN	TYP	MAX	UNIT
XOUT differential output voltage			1000		mVpp
XOUT common mode voltage			0.83		V

Control Interface

Table 8   I²C Address selection

MA1	MA0	ADD input voltage
0	0	0 V ~ 0.1 VDD
0	1	Open
1	0	0.4 VDD ~ 0.6 VDD
1	1	0.9 VDD ~ VDD

Table 9   I²C bus characteristics

(VDD = 3 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	Test Condition	MIN	TYP	MAX	UNIT
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time between START and STOP Condition	t_{BUF}		1.3			µs
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	$T_{HD, STA}$		0.6			µs
LOW Period of SCL Clock	t_{LOW}		1.3			µs
HIGH Period of SCL Clock	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU,DAT}$		100			ns
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
SCL and SDA Rise and Fall Time	t_f,t_f				300	ns
Setup Time for a Repeated START Condition	$t_{SY,STA}$		0.6			µs
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Capacitive Load for each Bus Line	C_B				400	pF
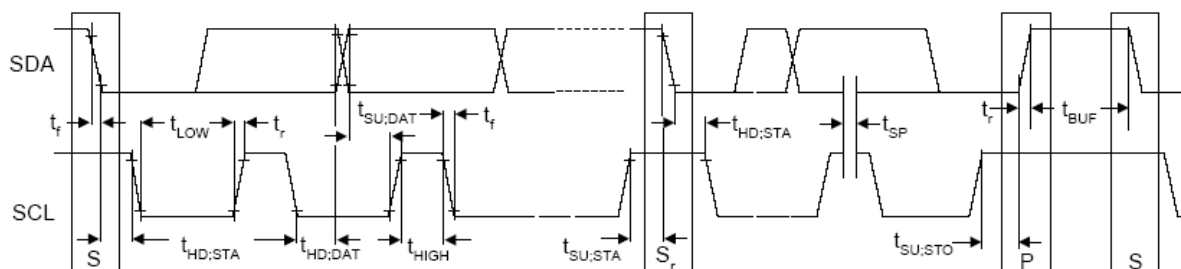
I²C Timing Diagram

Package Outline

| DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.130	.136	.140	3.30	3.45	3.55
E	.193	.197	.201	4.90	5.00	5.10
E1	.130	.136	.140	3.30	3.45	3.55
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		
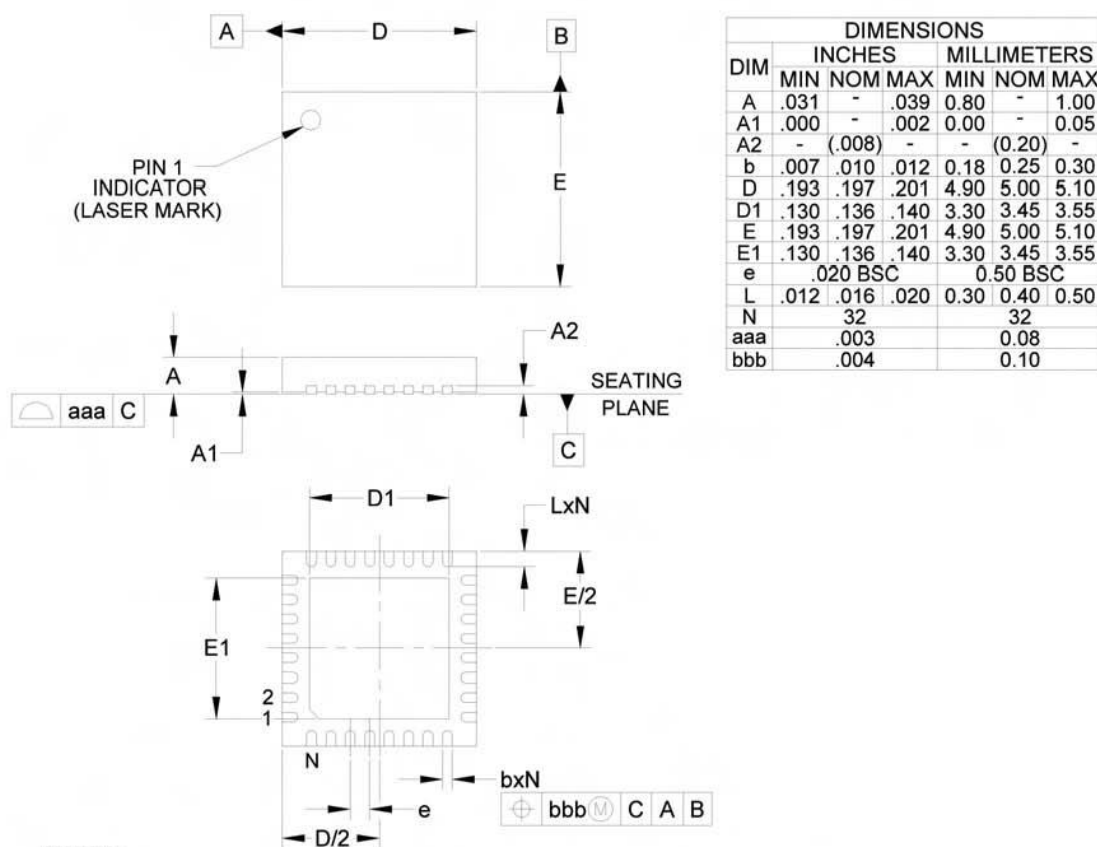
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

32-Pin 5x5 Quad Flat No-Lead (QFN)

Solder Mounting Condition
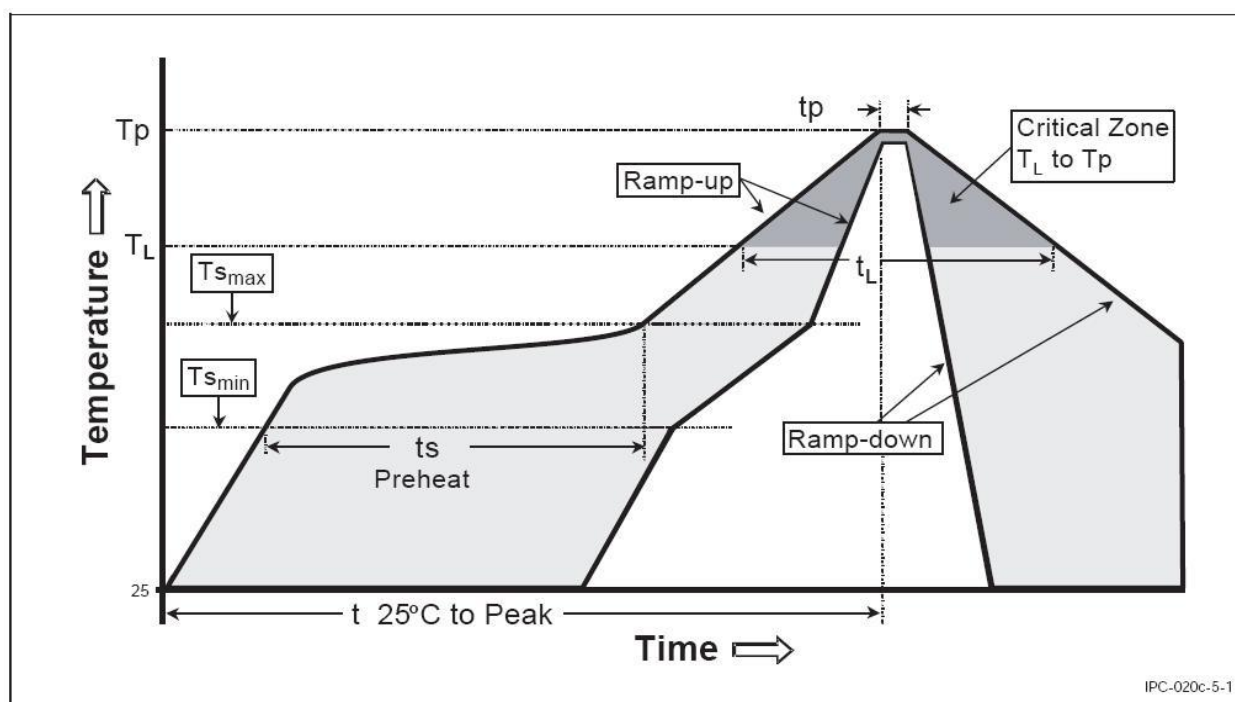
Classification Reflow Profile

Table-I Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 ^{o}C/second max.	3 ^{o}C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	100 ^{o}C 100 ^{o}C 60-120 seconds	150 ^{o}C 200 ^{o}C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	183 ^{o}C 60-150seconds	217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 ^{o}C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ^{o}C/second max.	6 ^{o}C/seconds max.

Time 25 ^{o}C to Peak Temperature	6 minutes max.	8 minutes max.

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
＜2.5mm	240 + 0/-5 ^{o}C	225 + 0/-5 ^{o}C
≥2.5mm	225 + 0/-5 ^{o}C	225 + 0/-5 ^{o}C

Table – III Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 ＜350	Volume mm^3 350-2000	Volume mm^3 ＞2000
＜1.6mm	260 + 0 ^{o}C *	260 + 0 ^{o}C *	260 + 0 ^{o}C *
1.6mm – 2.5mm	260 + 0 ^{o}C *	250 + 0 ^{o}C *	245 + 0 ^{o}C *
≥2.5mm	250 + 0 ^{o}C *	245 + 0 ^{o}C *	245 + 0 ^{o}C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ^{o}C. For example 260+ 0 ^{o}C) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ^{o}C, - X ^{o}C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 ^{o}C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a "lead-free" assembly process **shall** be evaluated using the "lead free" classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

RDA Microelectronics, Inc.
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